

PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of:

Tim J. Corbett

Serial No.: 09/928,314

Filed: August 13, 2001

For: LASER MARKING TECHNIQUES

Confirmation No.: 7920

Examiner: G. Fourson, III

Group Art Unit: 2823

Attorney Docket No.: 2269-2688.5US

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APPEAL BRIEF

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Attention: Board of Patent Appeals and Interferences

Sirs:

This brief is submitted in TRIPLICATE pursuant to 37 C.F.R. § 1.192(a) and in the format required by 37 C.F.R. § 1.192(c) and with the fee required by 37 C.F.R. § 1.17(c).

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(1) REAL PARTY IN INTEREST

U.S. Serial No. 09/928,314, the application at issue in the above-referenced appeal, has been assigned to Micron Technology, Inc. The assignment has been recorded with the United States Patent & Trademark Office (hereinafter the "Office") Reel No. 7841, Frame No. 0079. Accordingly, Micron Technology, Inc. is the real party in interest to the referenced appeal.

(2) RELATED APPEALS AND INTERFERENCES

The undersigned attorney is not aware of any action, including any appeals or interferences, that is currently ongoing before Board of Patent Appeals and Interferences in any application which is related to the above-referenced application and that may affect or be affected by the Board's decision in the appeal of the status of the above-referenced application.

(3) STATUS OF CLAIMS

Claims 1-23 remain pending in the above-referenced application, each standing rejected.

No claims have been allowed.

The rejections of claims 1-23 are being appealed.

(4) STATUS OF AMENDMENTS

The above-referenced application was filed on August 13, 2001, with twenty-three (23) claims.

On October 17, 2001, a Preliminary Amendment was filed. Revisions to claims 5, 13, 22, and 23 were presented in the Preliminary Amendment.

A first Office Action on the merits was mailed on December 17, 2002. All of the pending claims were rejected in that Office Action. In an Amendment dated March 17, 2003, claims 1, 5, 7, 11, 13, 17, 19-21, 22, and 23 were amended; these amendments being the last claim amendments in the above-referenced application. The Amendment of March 17, 2003, also provided explanations as to the patentability of each of claims 1-23 over the art that had been relied upon the rejections presented in the Office Action of December 17, 2002.

On June 9, 2003, a Final Office Action was mailed. The previous grounds for rejecting claims 1-23 were withdrawn, but new grounds for rejecting each of these claims were asserted. On July 31, 2003, an Amendment Under 37 C.F.R. § 1.116 was filed, responsive to the Final Office Action. While revisions to the specification were presented in the Amendment Under 37 C.F.R. § 1.116, no further revisions were made to the claims. Additionally, the Amendment Under 37 C.F.R. § 1.116 including reasoning in support of the patentability of each of claims 1-23.

Nonetheless, the rejections of claims 1-23 were maintained in an Advisory Action dated October 14, 2003.

Thereafter, on October 20, 2003, a Notice of Appeal was filed.

This Appeal Brief follows the Notice of Appeal. As this Appeal Brief is being filed by Monday, December 22, 2003, it should be deemed to have been filed within two months of the filing date of the Notice of Appeal, as December 20, 2003, fell on a Saturday. 37 C.F.R. § 1.7.

(5) SUMMARY OF THE INVENTION

The invention disclosed in the above-referenced application and recited in the claims thereof includes a method of laser marking a surface of a semiconductor chip, bare or packaged, once the semiconductor chip has been characterized for use. *See, e.g.*, paragraphs [0004] and [0006]. Such marking may be effected without creating a visible imprint in the surface of the semiconductor chip.

In one embodiment of the invention, regions of the surface of a bare or packaged semiconductor chip that is to be marked are heated with a laser. *See, e.g.*, paragraph [0012]. A laser-reactive substance reacts with these heated areas to form the desired markings on the surface of the bare or packaged semiconductor chip. *See, id.* These markings are bonded or otherwise secured onto the surface of the bare or packaged semiconductor chip. *See, e.g., id.* In forming a marking on the surface of a bare or packaged semiconductor chip, the method of the invention does not substantially etch, imprint, or otherwise alter the surface of the bare or packaged semiconductor chip itself. *See id.*

(6) ISSUES

The Examiner's positions on the following issues are being appealed in the above-referenced application:

(A) Whether, under 35 U.S.C. § 103(a), claims 1-18 are nonobvious and, thus, patentable over the subject matter taught in U.S. Patent 4,594,263 to Folk (hereinafter "Folk"), in view of teachings from U.S. Patent 5,757,313 to Meneghini et al. (hereinafter "Meneghini"); and

(B) Whether, claims 19-23 are allowable under 35 U.S.C. § 103(a) for reciting subject matter which is nonobvious over that taught in Folk, in view of the teachings of Meneghini and, further, in view of teachings from U.S. Patent 5,256,578 to Corley et al. (hereinafter "Corley").

(7) GROUPING OF CLAIMS

Claims 1-23 should be grouped together. Claim 1 appear to be the most generic of this group. Claims 2-23 stand and fall with claim 1 and claims 1-18 fall with claim 1, but claims 19-23 do not.

(8) ARGUMENT

Claims 1-23 have been rejected under 35 U.S.C. § 103(a).

(A) Applicable Law

M.P.E.P. § 706.02(j) sets forth the standard for a rejection under 35 U.S.C. § 103(a):

To establish a *prima facie* case of obviousness, three basic criteria must be met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or combine reference teachings. Second, there must be a reasonable expectation of success. Finally, the prior art reference (or references when combined) must teach or suggest all the claim limitations. The teaching or suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art, and not based on applicant's disclosure. *In re Vaeck*, 947 F.2d 488, 20 USPQ2d 1438 (Fed. Cir. 1991).

(B) Reference Teachings

Folk

Folk teaches a process for marking semiconductor devices that have been packaged in metal. The process taught in Folk includes cleaning the surface of the metal package, using electroless plating techniques to form a nickel layer thereon, cleaning residual salts from the metal package and the nickel layer, and exposing the nickel to acid to convert it to an optically black form which is highly absorptive of laser energy. When marking is desired, such as when a semiconductor device package has been tested and it is determined that the semiconductor device is suitable for use, selected locations of the optically black coating on the nickel layer may be exposed to a laser to expose the underlying, shiny nickel at those locations, thereby forming a mark on the metal semiconductor device package.

Folk prominently teaches that, because inks and other materials must be dried or cured, such materials undesirably “involve several stages of handling” and result in marks that “may be removed by abrasion.” Col. 1, lines 28-30. Folk also teaches that, due to these inadequacies in ink and polymer marking processes, the processes disclosed in Folk are far superior to the use of inks or other similar materials that require drying or curing.

Menghini

Menghini teaches inks that may be applied to various types of substrates, including microelectronic devices (col. 1, lines 12-15), and that require curing by laser irradiation. *Id.*

(C) Analysis

Claims 1-18 have been rejected under 35 U.S.C. § 103(a) for purportedly reciting subject matter which is unpatentable over that taught in Folk, in view of the teachings of Meneghini.

Claims 19-23 stand rejected under 35 U.S.C. § 103(a) for purportedly reciting subject matter which is unpatentable over the combination teachings from Folk, in view of teachings from Meneghini, purported prior art admissions that have been made in the above-referenced application (hereinafter “PPA”), and the teachings Corley.

(i) Folk in View of Menghini

It is respectfully submitted that a *prima facie* case of obviousness under 35 U.S.C. § 103(a) cannot be established against any of claims 1-18 based on the teachings of Folk and Menghini.

A *prima facie* case of obviousness under 35 U.S.C. § 103(a) cannot be established against any of the claims of the above-referenced application because Folk clearly teaches away from the asserted combination of teachings thereof with the type of teachings provided by Menghini.

In particular, combining teachings from Folk in Menghini in the manner that has been asserted by the Office would require modifying the nickel coating and laser marking process taught in Folk by using ink or polymers, as taught in Menghini, in place of the nickel coating. Specifically, Folk teaches that the use of ink and, presumably, other polymers, for marking is undesirable since several stages of handling may be required, cure times are required, and such marks may be removed from substrates. Col. 1, lines 25-31. Thus, Folk strongly discourages the

use of materials of the type taught in Menghini in place of the nickel coating of Folk, thereby teaching away from this asserted combination of reference teachings.

As Folk teaches that the teachings thereof may not be combined with teachings of the type made in Menghini, it is respectfully submitted that the only way that one of ordinary skill in the art would have been motivated to combine the teachings of Folk and Menghini would have been from improper hindsight provided by the teachings of the above-referenced application.

It is, therefore, respectfully submitted that a *prima facie* case of obviousness under 35 U.S.C. § 103(a) has not been established against any of claims 1-18.

(ii) Folk, Menghini, and Corley

Claims 19-23 are allowable, among other reasons, as depending either directly or indirectly from independent claim 13, which is allowable.

It is further submitted that neither the PPA nor the teachings of Corley would have convinced one of ordinary skill in the art to ignore the fact that Folk teaches away from the combination of teachings thereof with teachings from Menghini.

Therefore, a *prima facie* case of obviousness under 35 U.S.C. § 103(a) has not been established against any of claims 19-23.

For these reasons, it is respectfully requested that the 35 U.S.C. § 103(a) rejections of claims 1-23 be reversed.

(9) APPENDIX

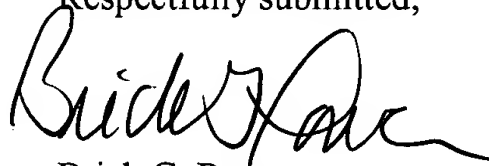
The Appendix to this Appeal Brief includes a listing of claims 1-23 as they currently stand.

(10) CONCLUSION

It is respectfully submitted that claims 1-18 are nonobvious and, thus, patentable under 35 U.S.C. § 103(a) over the subject matter taught in Folk, in view of teachings from Meneghini, and that claims 19-23 are allowable under 35 U.S.C. § 103(a) for reciting subject matter which is nonobvious over that taught in Folk, in view of the teachings of Meneghini and, further, in view of teachings from Corley.

For these reasons, reversal of the 35 U.S.C. § 103(a) rejections is respectfully requested.

Respectfully submitted,



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Date: December 23, 2003
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APPENDIX

1. (Previously presented) In a method of producing semiconductor chips wherein the chips are at least fabricated and characterized, the improvement comprising:
marking with identifying indicia only those chips which are characterized for use by exposing
selected locations of at least one of a surface of at least one semiconductor chip and an
energy-reactive marking material to energy to cause said energy-reactive marking
material to adhere to said surface.
2. The method of claim 1, wherein said marking is effected following packaging of the
chips.
3. The method of claim 1, wherein said marking is effected as the last step in the
production process.
4. The method of claim 1, wherein said marking comprises laser marking.
5. (Previously presented) The method of claim 1, wherein said marking comprises:
providing said energy-reactive marking material over said surface of said at least one
semiconductor chip.
6. The method of claim 5, wherein said exposing is effected without substantially
creating an imprint in said surface.

7. (Previously presented) A method for producing semiconductor chips, comprising:
fabricating at least one semiconductor chip;
determining whether said at least one semiconductor chip is suitable for use; and
marking said at least one semiconductor chip only if said at least one semiconductor chip is
determined to be suitable for use by exposing selected locations of at least one of a
surface of said at least one semiconductor chip and an energy-reactive marking material
to energy to cause said energy-reactive marking material to adhere to said surface.
8. The method of claim 7, further comprising packaging said at least one semiconductor
chip.
9. The method of claim 7, wherein said marking is effected as the last step in the
production process.
10. The method of claim 7, wherein said marking comprises laser marking.
11. (Previously presented) The method of claim 7, wherein said marking comprises:
providing said energy-reactive marking material over at least a portion of said surface of said at
least one semiconductor chip.

12. The method of claim 11, wherein said exposing is effected without creating an imprint in said surface.

13. (Previously presented) A method for producing semiconductor chips, comprising:
providing at least one semiconductor chip which has been characterized as suitable for use and at least one semiconductor chip which has been characterized as unsuitable for use; and
marking with identifying indicia only said at least one semiconductor chip which has been characterized as suitable for use by exposing selected locations of at least one of a surface of said at least one semiconductor chip and an energy-reactive marking material to energy to cause said energy-reactive marking material to adhere to said surface.

14. The method of claim 13, wherein said providing comprises providing at least one packaged semiconductor chip which has been characterized as suitable for use and at least one packaged semiconductor chip which has been characterized as unsuitable for use.

15. The method of claim 13, wherein said marking is effected as the last step in the production process.

16. The method of claim 13, wherein said marking comprises laser marking.

17. (Previously presented) The method of claim 13, wherein said marking comprises: providing said energy-reactive marking material over at least a portion of said surface of said at least one semiconductor chip which has been characterized as suitable for use.

18. The method of claim 17, wherein said exposing is effected without forming an imprint in said surface.

19. (Previously presented) The method of claim 13, further comprising comparing said identifying indicia to an identifying indicia model.

20. (Previously presented) The method of claim 19, further comprising determining whether said identifying indicia substantially matches said identifying indicia model.

21. (Previously presented) The method of claim 20, further comprising rejecting said at least one semiconductor chip which has been characterized as suitable for use if its respective identifying indicia does not substantially match said identifying indicia model.

22. (Previously presented) The method of claim 21, further comprising removing said identifying indicia which does not substantially match said identifying indicia model from said at least one rejected semiconductor chip which has been characterized as suitable for use.

23. (Previously presented) The method of claim 22, further comprising remarking said at least one rejected semiconductor chip which has been characterized as suitable for use.



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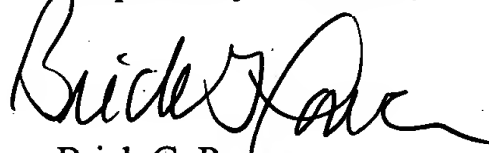
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For these reasons, reversal of the 35 U.S.C. § 103(a) rejections is respectfully requested.

Respectfully submitted,



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APPENDIX

1. (Previously presented) In a method of producing semiconductor chips wherein the chips are at least fabricated and characterized, the improvement comprising:
marking with identifying indicia only those chips which are characterized for use by exposing selected locations of at least one of a surface of at least one semiconductor chip and an energy-reactive marking material to energy to cause said energy-reactive marking material to adhere to said surface.
2. The method of claim 1, wherein said marking is effected following packaging of the chips.
3. The method of claim 1, wherein said marking is effected as the last step in the production process.
4. The method of claim 1, wherein said marking comprises laser marking.
5. (Previously presented) The method of claim 1, wherein said marking comprises:
providing said energy-reactive marking material over said surface of said at least one semiconductor chip.
6. The method of claim 5, wherein said exposing is effected without substantially creating an imprint in said surface.

7. (Previously presented) A method for producing semiconductor chips, comprising:
fabricating at least one semiconductor chip;
determining whether said at least one semiconductor chip is suitable for use; and
marking said at least one semiconductor chip only if said at least one semiconductor chip is
determined to be suitable for use by exposing selected locations of at least one of a
surface of said at least one semiconductor chip and an energy-reactive marking material
to energy to cause said energy-reactive marking material to adhere to said surface.
8. The method of claim 7, further comprising packaging said at least one semiconductor
chip.
9. The method of claim 7, wherein said marking is effected as the last step in the
production process.
10. The method of claim 7, wherein said marking comprises laser marking.
11. (Previously presented) The method of claim 7, wherein said marking comprises:
providing said energy-reactive marking material over at least a portion of said surface of said at
least one semiconductor chip.

12. The method of claim 11, wherein said exposing is effected without creating an imprint in said surface.

13. (Previously presented) A method for producing semiconductor chips, comprising:
providing at least one semiconductor chip which has been characterized as suitable for use and at least one semiconductor chip which has been characterized as unsuitable for use; and
marking with identifying indicia only said at least one semiconductor chip which has been characterized as suitable for use by exposing selected locations of at least one of a surface of said at least one semiconductor chip and an energy-reactive marking material to energy to cause said energy-reactive marking material to adhere to said surface.

14. The method of claim 13, wherein said providing comprises providing at least one packaged semiconductor chip which has been characterized as suitable for use and at least one packaged semiconductor chip which has been characterized as unsuitable for use.

15. The method of claim 13, wherein said marking is effected as the last step in the production process.

16. The method of claim 13, wherein said marking comprises laser marking.

17. (Previously presented) The method of claim 13, wherein said marking comprises: providing said energy-reactive marking material over at least a portion of said surface of said at least one semiconductor chip which has been characterized as suitable for use.

18. The method of claim 17, wherein said exposing is effected without forming an imprint in said surface.

19. (Previously presented) The method of claim 13, further comprising comparing said identifying indicia to an identifying indicia model.

20. (Previously presented) The method of claim 19, further comprising determining whether said identifying indicia substantially matches said identifying indicia model.

21. (Previously presented) The method of claim 20, further comprising rejecting said at least one semiconductor chip which has been characterized as suitable for use if its respective identifying indicia does not substantially match said identifying indicia model.

22. (Previously presented) The method of claim 21, further comprising removing said identifying indicia which does not substantially match said identifying indicia model from said at least one rejected semiconductor chip which has been characterized as suitable for use.

23. (Previously presented) The method of claim 22, further comprising remarking said at least one rejected semiconductor chip which has been characterized as suitable for use.